Amend claim 2 as follows:

--2. (amended) The semiconductor memory device according to claim 6, wherein said metal is a refractory metal, and said first contact further includes a barrier layer formed between said source and said first metal portion.--

Amend claim 3 as follows:

--3. (amended) The semiconductor memory device according to claim 2, wherein said refractory metal is tungsten, and said barrier layer is formed of titanium nitride.--

Amend claim 6 as follows:

--6. (amended) A semiconductor memory device comprising:

a substrate;

a MOS (metal oxide semiconductor) transistor formed in a surface portion of said substrate, wherein said MOS transistor includes a source, a gate, and a drain;

a first inter-level dielectric covering said MOS transistor;

a capacitor element including:

a bottom electrode,

a dielectric layer formed on said bottom electrode, and

an upper electrode formed on said dielectric layer;

a first contact formed through said first inter-level dielectric to electrically connect said bottom electrode to said source, wherein said first contact includes a first metal portion formed of metal; and

a second contact formed through said first inter-level dielectric to be connected to said drain, wherein said second contact includes a second metal portion formed of said metal.--

Amend claim 10 as follows:

--10. (amended) The semiconductor memory device according to claim 6, wherein said bottom electrode comprises:

a polysilicon layer connected to said dielectric layer, and

an electrode barrier layer formed between said first metal portion and said polysilicon layer.--

Cancel claim 13.

Add the following new claims:

--23. (new) A semiconductor memory device, comprising:

a substrate;

a transistor in a surface of said substrate, said transistor having a source, drain, and gate;

a first inter-level dielectric on said transistor;

a second inter-level dielectric on said first inter-level dielectric;

a capacitor element that extends through said second

inter-level dielectric, said capacitor element having bottom and top electrodes and a capacitor dielectric therebetween;

a bit line contact plug that extends through said second inter-level dielectric;

a first contact through said first inter-level dielectric that connects said bottom electrode of said capacitor element to said source of said transistor; and

a second contact through said first inter-level dielectric that connects said bit line contact plug to said drain of said transistor,

wherein said first and second contacts and said bit line contact plug are all formed of a same first metal.

--24. (new) The device of claim 23, wherein the first metal is tungsten.

--25. (new) The device of claim 23, further comprising a barrier layer between said bottom electrode of said capacitor element and said second inter-level dielectric, said barrier layer extending only partially along said capacitor element so that a portion of said bottom electrode directly contacts said second inter-level dielectric.--

REMARKS

The specification, drawings, and claim 3 have been amended to make editorial changes therein, bearing in mind the